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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/052,736
Filing Date: January 23, 2002
Appellant(s): IKEDA, SATOSHI

Ronald P. Kananen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/12/2007 appealing from the Non-Final Office action mailed 2/7/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Non-Final

The appellant's statement of the status of amendments after non-final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Reichert (US Patent No. 6,553,529), filed: July 23, 1999.

Regarding independent Claims 6, 22, Reichert discloses a semiconductor testing apparatus and method, Fig. 1, wherein an input signal of a test pattern from a pattern generation circuit 24 is supplied to a semiconductor device-under-test (DUT) 28 and an output signal obtained from the DUT 28 is compared with a prescribed expected in a failure processing circuit 50, comprising:

Test pattern memory means (a pattern memory) in a workstation 22, which operates as a test controller having a pattern memory and a user interface and a pattern generation circuit having respective high-speed and low-speed modes for selectively

producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. A system bus connects to the test controller and the pattern generation circuit for routing command and data signals, Summary of the Invention and Fig. 1.

Test pattern generation means (pattern generator 24) for producing test patterns for application to the device-under-test 28. The pattern generator includes N pattern generators (only one shown in FIG. 1 for clarity) to generate a plurality of tester operating modes. The modes correspond to relatively high-speed (>250 MHz) and relatively slow-speed (<250 MHz) test patterns. A pin data line 27 and a global time set address line 29 are couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26.

Control means (test controller 22) for controlling the (pattern memory) and the (pattern generator 24) though the system bus 26, which connects to the test controller and the pattern generator for routing command and data signals. A timing system 30 includes producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28.

Wherein the pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed, which corresponds to the narrow cycle period rate, is grater than a predetermined rate (>250 MHz). Fig. 3 illustrates a high-speed test waveform suitable for application to a

high-speed DUT pin as defined by timing signals generated by the timing system, and Fig. 5 further illustrates a portion of a multi-period waveform for application to a slow-speed DUT pin of around 200 MHz. The timing logic 34 includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claim 7, Reichert discloses decision means (failure processing circuit 50) to detect a failure within said semiconductor device DUT 28 by comparing an output test pattern signal received from the DUT with a first (test controller 22)

Regarding Claim 8, Reichert discloses control means (test controller 22) the programmable PLL-based master oscillator MOSC 40 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claim 9, Reichert discloses first test pattern (test controller 22) is located at an address within the test pattern memory means (pattern memory) included in the workstation 22.

Regarding Claim 10, Reichert discloses semiconductor device DUT 28 is tested during the test pattern cycle period (DUT cycle), Figs. 3 and 5.

Regarding Claims 11-14, 23-25, Reichert discloses pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed, which corresponds to the narrow

cycle period rate, is grater than a predetermined rate (>250 MHz). Fig. 3 illustrates a high-speed test waveform suitable for application to a high-speed DUT pin as defined by timing signals generated by the timing system, and Fig. 5 further illustrates a portion of a multi-period waveform for application to a slow-speed DUT pin of around 200 MHz. The timing logic 34 includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12.

Regarding Claims 15-21, 26-32, Reichert discloses pattern generator including N pattern generators (only one shown in Fig. 1) to generate a plurality of tester operating modes, corresponding to relatively high-speed (>250 MHz) and relatively slow-speed (<250 MHz) test patterns. A pin data line 27 and a global time set address line 29 couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26. The timing system 30 includes timing logic 34 responsive to an edgiest memory 36 for producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28.

Response to Arguments

Appellant's arguments in the Appeal Brief filed on 4/12/2007, with respect to the rejection of claims 6-32 under 35 U.S.C. 102(e) as being anticipated by Reichert (US Patent No. 6,553,529, have been fully considered but they are not persuasive.

In reference to independent claims 6, 22, and claims 10, 15, 26, drawn to a semiconductor testing apparatus and method, Appellant argues Reichert fails to disclose the timing logic 34 as being adapted to generate a timing signal and an address specifying signal. In response to Appellant's argument, Reichert discloses a timing system 30 including the timing logic 34, which receives data and address signals from the pattern generation circuit 24 via the global time-set address line 29 and data line 27, and then generates programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28. Clearly, the timing system 30 of Reichert is capable of producing timing signals proportional to the data and address signals for defining a tester waveform to verify the operability of DUT 28, as shown in Fig. 3 and 5. Furthermore, the recited limitation, of an address specifying signal, does not imply an address signal corresponding to a location of the semiconductor device to be tested, but rather a signal associated with a specific test pattern, as disclosed by Reichert defining the tester waveform, Fig. 3. Each transition (or "edge") of the test waveform corresponds to one or more timing signals issued by one or more of the edge generators EG0-EG12 from the timing logic 34, where each "EG" is equivalent to Appellant's address specifying signal.

Furthermore, in response to Appellant's argument that Reichert fails to disclose, the test controller 22 as being adapted to generate a timing signal and an address specifying signal, clearly, the test controller 22 is capable of producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42. Thus, the test

controller generates command and data signals routed via a system bus for controlling the pattern generation circuit for generating test patterns including data and address signals on lines 27 and 29, respectively, for application to a device-under-test. Furthermore, the recited limitation, of control means being adapted to generate a timing signal and an address specifying signal, does not imply that the control means generates a test pattern associated with an address, but rather "the control means 110 controls the timings to generate the timing signal and the address specifying signal" as described in the Appellant's specification. Also, the specification describes, "control means 110 for controlling both the whole apparatus and a timing to generate a test pattern", which clearly indicates the purpose of the control means is to control the generation of the test pattern. Evidently, Reichert's test controller 22 is capable of generating timing and control signals coupled to the pattern generation circuit 24 via system bus 26 capable of generating data and address signals on lines 27 and 29 coupled to the timing system 30 including the timing logic 34 for producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42.

Appellant argues Reichert fails to disclose, the pattern generation circuit 24 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period. In response to Appellant's argument, the pattern generation circuit 24 is capable of generating test patterns including data and address signals on lines 27 and 29, respectively, in response to command and data signals generated from the test controller 22 routed via the system bus for controlling the pattern generation

circuit for generating test pattern corresponding to a test waveform having a DUT period of operation, such as the test pattern cycle period, as shown in Fig. 3.

In reference to Claim 7, in response to Appellant's argument, Reichert discloses a failure processing circuit 50 for detecting a failure within the semiconductor device DUT 28 by comparing an output test pattern signal received from the DUT with an expected pattern stored in a memory area in the test controller 22. The location of the expected pattern is not critical in detecting a failure, since the failure processing circuit 50 is capable of detecting a failure by comparing the DUT output results with and expected pattern regardless of its location.

In reference to Claim 8, in response to Appellant's argument that Reichert fails to disclose, the computer workstation 22 as being adapted to vary the duration of the test pattern cycle period, Reichert discloses a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 in the timing logic that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12. Control of the edge generators is carried out by pre-programming the test controller 22 and the edge set memory 36 to fire predetermined edge generators at the specific increments of time following the beginning of the DUT cycle (BOC). Clearly, test controller 22 is capable of controlling the duration of the test pattern cycle period.

In reference to Claim 9, in response to Appellant's argument, Reichert discloses a test pattern associated with an address generated in the pattern generation circuit 24.

In reference to Claims 11-14, 23-25, in response to Appellant's argument that Reichert fails to disclose, the test controller 22 as being adapted to generate a timing

signal and an address specifying signal, Reichert discloses a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12. The pattern generator 24 having respective high-speed and low-speed modes for selectively producing test patterns according to the pattern memory for application to the device-under-test according to a DUT clock period. The high-speed corresponds to the narrow cycle period rate, Fig. 3, which illustrates a high-speed test waveform as defined by timing signals generated by the timing system, and Fig. 5 further illustrates a portion of a multi-period waveform for application to a slow-speed DUT pin.

In reference to Claims 16-21, 27-32, in response to Appellant's argument, Reichert discloses pattern generator including N pattern generators (only one shown in Fig. 1) to generate a plurality of tester operating modes, corresponding to relatively high-speed (>250 MHz) and relatively slow-speed (<250 MHz) test patterns. A pin data line 27 and a global time set address line 29 couple the pattern generator to the timing system while pattern information to and from the failure processor is distributed via the system bus 26. The timing system 30 includes timing logic 34 responsive to an edgiest memory 36 for producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42 at predetermined timings (defining a tester waveform) with respect to a period of operation for a device-under-test (DUT) 28.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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